September 2021

COMPUTER ORGANISATION & ARCHITECTURE

Time Allowed: 1.5 Hours | Full Marks: 70

Answer to Question No.1 is compulsory and Answer any two questions from the rest.

1. Answer the following questions (any twenty): 20x2

Choose the correct answer from the given alternatives:

i. Assembly language-
(A) uses alphabetic codes in place of binary numbers used in machine language
(B) is the easiest language to write programs
(C) need not be translated into machine language
(D) None of these

ii. (2FAOC)16 is equivalent to-
(A) (195 084)10
(B) (0010111110100000 1100)2
(C) Both (A) and (B)
(D) None of these

iii. Which of the following architecture is/are not suitable for realizing SIMD?
(A)Vector Processor
(B) Array Processor
(C)Von Neumann
(D) All of the above

iv. Floating point representation is used to store-
(A) Boolean values
(B) whole numbers
(C) real integers
(D) integers

v. In signed-magnitude binary division, if the dividend is (11100)2 and divisor is (10011)2 then the result is-
(A) (00100)2
(B) (10100)2
(C) (11001)2
(D) (01100)2

vi. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be-
(A) (812)10
(B) (-12)10
(C) (12)10
(D) (-812)10

vii. Computers use addressing mode techniques for
(A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
(B) to reduce no. of bits in the field of instruction
(C) specifying rules for modifying or interpreting address field of the instruction
(D) All the above

viii. In a vectored interrupt.

(A) the branch address is assigned to a fixed location in memory.
(B) the interrupting source supplies the branch information to the processor through an interrupt vector.
(C) the branch address is obtained from a register in the processor
(D) none of the above

ix. A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit
(A) D T Qn = •
(B) D = T
(C) D = T . Qn
(D) D = T ⊕ Qn

x. How many different addresses are required by the memory that contain 16K words?
(A)16,380
(B) 16,382
(C)16,384
(D) 16,386

xi. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(A) 8
(B) 16
(C) 24

xii. SIMD represents an organization that _____.
(A) refers to a computer system capable of processing several programs at the same time.
(B) represents organization of single computer containing a control unit, processor unit and a memory unit.
(C) includes many processing units under the supervision of a common control unit
(D) none of the above.

Fill in the blanks:

xiii. When two equal numbers are subtracted, the result would be not_____.
xiv. Logic X-OR operation of (4ACO)H & (B53F)H results _____ .
xv. The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is _____ .
xvi. Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called _____ .
xvii. The cache memory of 1K words using direct mapping with a block size of 4 words _____ blocks can the cache accommodate.
xviii. The performance of cache memory is frequently measured in terms of a quantity called _____.

State whether the following statements are 'True' or 'False':

xix. Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers.
xx. An arithmetic shift left multiplies a signed binary number by 2.
xxi. DRAM can store data until the computer is powered down.
xxii. Content of Stack Pointer (SP) address of the top element of the stack.
xxiii. Laser printer is a type of Impact Printer.
xxiv. Access time of SRAM is faster than DRAM.
xxv. Instruction must be executed before the fetching.

2. a) Explain indirect address mode and how the effective address is calculated in this case.
b) What is wrong with the following register transfer statements?
i. xT : AR ←AR, AR ←0
ii. yT : $R_1 \leftarrow R_2$, $R_1 \leftarrow 0$
iii. zT : PC← AR, PC ← PC+1 7+8

3. a) Divide dividend (-53)10 by divisor (-7)10 by using binary division algorithm, Show all steps.
b) Write down an algorithm for adding and subtracting numbers in signed – 2's complement representation. 7.5+7.5

4. a) Construct an associative memory page table with the number of words equal to the number of blocks in the main memory.
b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from the main memory. The main memory size is 32 128 K × . (i) How many bits are there in the tag, index block and word fields of the address format? (ii) What is the size of the cache memory? 5+(5+5)

5. a) How many ROM chips are required to produce a memory capacity of 4000 bytes? How many address lines are required to access the 4000 bytes? How many of these addresses will be common to all these chips?
b) A Computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. (i) How many bits are there in the operation code, the register code part, and the address part? (ii) Draw the instruction word format and indicate the number of bits in each part. (iii) How many bits are there in the data and address inputs of the memory? (1+1+4)+(3+3+3)

6. a) Explain associative memory with the help of block diagram.
b) How page fault is handled by memory management software. 7.5+7.5

7. a) A virtual memory system has an address space of 8k words, memory space of 4k words and Page & Block size of 1k words. The following page reference changes occur during a given time interval.

4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7

b) Determine the four pages that are resident in main memory after each Page reference change if the replacement algorithm used is: (i) FIFO (ii) LRU.
Show the memory organization (1024 bytes) of a computer with four 128x8 RAM Chips and 512x8 ROM Chip. How many address lines are required to access memory? (3+3)+(7+2)

8. a) Give the cache access time as 10 ns memory access time as 100 ns and cache hit rate as 90%, calculate the effective memory access time.
b) Consider a cache (M1) and memory (M2) hierarchy with the following characteristics: M1 : 16 K words, 50 ns access time M2 : 1 M words, 400 ns access time Assume 8 words cache blocks and a set size of 256 words with set associative mapping. (i)Show the mapping between M2 and M1. (ii) Calculate the Effective Memory Access time with a cache hit ratio of h = .95.
c) A Virtual memory has a Page Size of 1K words. There are eight Pages and four blocks. The associative memory page table contains the following entries.

Page	Block
6	0
1	1
4	2
0	3

c) Give the list of virtual addresses in decimal that will cause a Page fault if used by CPU. 3+(4+3)+5

9. a) Justify the statement "Stack computer consists of an operation code only with no address field".
b) If a Computer has 128 operation codes and 512 k addresses, how many bits would be required for (i) Single address instruction (ii) Two address instruction.

c) What is the main difference between implied and immediate modes of addressing? 5+5+5

10. a) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.

b) Discuss Flynn's classification of computer 7.5+7.5

11. a) Explain Booths algorithm for multiplying two signed binary numbers with example.

b) Write a program by using two - addressing & one-addressing format to evaluate with an example.
A–B+C * (D-E)/ C + G * H 7.5+7.5
