March 2021

DIGITAL ELECTRONICS

Time Allowed: 3 Hours | Full Marks: 70

Answer to Question No.1 is compulsory and Answer any five questions from the rest.

1. Choose the correct answer from the given alternatives (any twenty): 20x1

i) In case of subtraction of two bits, the difference bit can be implemented by- a) 2-input AND gate, b) 2-input OR gate, c) 2-input XOR gate, d) 2-input XNOR gate.

ii) BCD-to-decimal decoder has- a) 10 inputs and 10 outputs,b) 4 inputs and 10 outputs,c) 10 inputs and 4 outputs,d)1 input and 10 outputs.

iii) K-map method of simplification can only be applied when the given Boolean function is in- a) Canonical form, b) SOP form, c) POS form, d) all of the above.

iv) In octal system the value $2^9$is- a) 100,b) 1000,c) 90,d) 600.

v) A ring counter is a-a) shift register, b) Synchronous counter, c) up-down counter, d) none of the above.

vi) A 5 KHz clock signal having a duty cycle 25% is used to clock a 2-bit binary ripple counter. What will be the frequency and duty cycle of the output of the MSB flip-flop?- a) 1.25 KHz, 50% b) 1.25 KHz, 25% c) 2.5 KHz, 50% d) 2.5 KHz, 75%.

vii) A MOD-32 binary synchronous counter would require- a) 6 flip-flops and 4 AND gates, b) 5 flip-flops and 3 AND gates, c) 5 flip-flops and 4 AND gates, d) 4 flip-flops and 2 AND gates.

viii) Which of the following gate can be used as a controlled inverter?- a) AND, b) OR, c) XOR, d) NAND.

ix) Out of the following, the fastest A/D converter type is- a) simultaneous A/D converter, b)counter type A/D converter, c) successive approximation type A/D converter, d) dual-slope type A/D converter.

x) The programmable logic device having a programmable AND-array at the input and programmable OR-array at the outputis called a- a) PLA, b) PAL, c) PGA, d)FPGA.

xi) Type of RAM in which data is stored in the form of charge on a capacitor is- a) Asynchronous SRAM, b) synchronous SRAM, c) DRAM, d) All of these.

xii) Identify the volatile memory-a) EPROM, b) PROM, c) SRAM, d)Flash memory.

xiii) To build a mod-99 counter the number of flip-flop required is-a) 5, b)6, c)7, d)100.

xiv) Which of the following does not represent Boolean algebra operation?- a) AND, b) OR, c) NOT, d) XOR.

xv) SRAM is to be used as- a) main memory, b) virtual memory, c) cache memory,d) auxiliary memory.

xvi) A divide-by-78 counter is realized by using-a) six mod-13 counters, b) thirteen mod-6 counters, c) one mod-13 counter followed by one mod-6 counter, d)thirteen mod-13 counters.

xvii) A 5-bit Johnson counter is a- a) Divide-by-32 counter, b) Divide-by-10 counter, c) Divide-by-16 counter, d) Divide-by-5 counter.

xviii) Any given truth table can be represented by a-a) K-map, b) SOP form, c) POS form, d) all of the above.

xix) In 2's complement system 10000 is equivalent to- (a) -0, (b) -15, (c) +16, (d) -16.

xx) The switching speed of ECL is very high because- (a) The transistors are switched between cut-off and saturation regions, (b) The transistors are switched between active and saturation regions, (c) The transistors are switched between cut-off and active regions, (d) the transistors may operate in any of above three regions.

xxi) Which of the following consumes the list power?- (a) TTL, (b) ECL, (c) CMOS, (d) Low power TTL.

xxii) A digital voltmeter has- a) digital input & digital output, b) digital input &analog output, c) analog input & digital output, d) analog input &analog output.

xxiii) In a two variable Boolean expression, a group of four 1's in the corresponding K-map will yield a term having- a) 1 literal, b) 2 literals, c) 3 literals, d) none of the above.

xxiv) (A + B.C) (A + B' + C') would simplify to- a) A, b) A + B' + C', c) A + B.C, d) A.B.C.

xxv) Which of the following 4-bit combination is invalid BCD?-a)0101,b) 1010,c)1001,d)0111.

2. What is T flip-flop? Show how J-K F/F can be converted into S-R F/F. 2+8

3. Design a modulo-5 ripple (asynchronous) up-counter with JK flip. What is meant by the term asynchronous inputs of Flip-Flop? 8+2

4. Draw the block diagram of 4 bit shift-right PISO register and briefly explain its operation.What is FPGA? 8+2

5. Explain the working principle of Dual slope type A/D convertor with the help of necessary diagram. What is step size in DAC? 8+2

6. What are the major advantages of ECL logic? Why is a pull-up resistor needed when connecting TTL logic to CMOS logic? Briefly explain the operation of NMOS inverter with the help of circuit diagram. 3+2+5

7. Describe a basic ECL NOR gate and explain its working in short with the help of truth table and diagram? Why CMOS is used in VLSI? (2+2+3+1)+2

8. a) Perform the following conversion: (i) $(0.513)10 = (?)_8$ (ii) $(59.57)8 = (?)_2$.
   b) State the associative property of Boolean algebra? What is canonical POS? (2½+2½)+(3+2)

9. Simplify the following expression using K-map and implement the simplified expression using NOR gates only: $f(x1, x2, x3, x4) = \Sigma m(4, 6, 8, 10, 11, 12, 15) + d(3, 5, 7, 9)$. 5+5

10. a) Draw the Half Subtractor circuit using only two input NAND gate.
    b) Use Karnaugh map to find the minimum-cost POS expressions for the function $f(x_1,...,x_4) = x_1'x_3'x_4' + x_3x_4 + x_1'x_2'x_4 + x_1x_2x_3'x_4$ assuming that there are also don't-cares defined as D = (9, 12, 14). 3+7